Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-46 (Canceled).

Claim 47 (Currently Amended): A method of manufacturing a semiconductor device comprising:

forming a first gate electrode and a second gate electrode on a semiconductor substrate;

forming a diffusion layer, with the first gate electrode as a mask

forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first gate electrode~~;~~ and said second gate electrode ~~and said diffusion layer~~ in such a manner that a portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height ~~equal to~~ above a height of said first gate electrode ~~or above, another portion of said first insulating film is provided on a major part of said diffusion layer to a height lower than a height of said first gate electrode and a further portion of said first insulating film is provided on a minor part of said diffusion layer to a height equal to a height of said first gate electrode or above;~~

forming a second insulating film on said first insulating film;

forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film;

etching a portion of said first insulating film, a portion of said second insulating film and a portion of said interlayer insulating film, which are on said

major part of said diffusion layer, to form a contact hole leading to said major part of said diffusion layer; and

embedding a conductive material in said contact hole to form a contact electrode connected to said major part of said diffusion layer.

Claim 48 (Currently Amended): A method of manufacturing a semiconductor device comprising:

forming, on a semiconductor substrate, a plurality of first memory cell gates, a pair of first selecting gates sandwiching said first memory cell gates, a plurality of second memory cell gates and a pair of second selecting gates sandwiching said second memory cell gates;

forming a plurality of diffusion layers in said semiconductor substrate while using as masks said first memory cell gates, said pair of first selecting gates, said second memory cell gates and said pair of second selecting gates;

forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first memory cell gates, said second memory cell gates and said diffusion layers in such a manner that portions of said first insulating film are embedded between said first memory cell gates ~~and~~ or between said second memory cell gates, a portion of said first insulating film is provided on one of said diffusion layers, on which one of said pair of first selecting gates is adjacent to one of said pair of second selecting gates in such a manner that a part of said portion of said first insulating film, which is on a major part of said one of said diffusion layers, has a thickness thinner than a thickness of said portions of said first insulating film, which are embedded between said first memory cell gates and between said second memory cell gates;

forming a second insulating film on said first insulating film;

forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film;

etching a portion of said first insulating film, a portion of said second insulating film and a portion of said interlayer insulating film, which are on said major part of said one of said diffusion layers, to form a contact hole leading to said major part of said one of said diffusion layers; and

embedding a conductive material in said contact hole to form a contact electrode connected to said major part of said one of said diffusion layers.

Claim 49 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said first insulating film is formed to cover said diffusion layer.

Claim 50 (New): The method of manufacturing a semiconductor device according to claim 47, wherein a density of hydrogen contained in said first insulating film is smaller than a density of hydrogen contained in said second insulating film.

Claim 51 (New): The method of manufacturing a semiconductor device according to claim 47, wherein a density of trap with respect to electric charge existing in said first insulating film is smaller than a density of trap with respect to electric charge existing in said second insulating film.

Claim 52 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said first insulating film is made of a material selected from a group including silicon oxide, oxy-nitride and oxidized silicon nitride.

Claim 53 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said second insulating film is made of silicon nitride.

Claim 54 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said first insulating film contains a void.

Claim 55 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said interlayer insulating film contains a void.

Claim 56 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height equal to a height of said first gate electrode and said second gate electrode.

Claim 57 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height in a middle of a height of said first gate electrode and said second gate electrode.

Claim 58 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said portion of said first insulating film is provided on side surfaces of said first gate electrode and said second gate electrode.

Claim 59 (New): The method of manufacturing a semiconductor device according to claim 47, wherein a further portion of said first insulating film is formed on upper surfaces of said first gate electrode and said second gate electrode.

Claim 60 (New): The method of manufacturing a semiconductor device according to claim 47, wherein said contact electrode is formed in a self-align manner to said first gate electrode.

Claim 61 (New): The method of manufacturing a semiconductor device according to claim 48, wherein a width of said one of said diffusion layers is larger than a width of each of those of said diffusion layers which are between said first memory cell gates or between said second memory cell gates.

Claim 62 (New): The method of manufacturing a semiconductor device according to claim 48, wherein a density of hydrogen contained in said first insulating film is smaller than a density of hydrogen contained in said second insulating film.

Claim 63 (New): The method of manufacturing a semiconductor device according to claim 48, wherein a density of trap with respect to electric charge existing in said first insulating film is smaller than a density of trap with respect to electric charge existing in said second insulating film.

Claim 64 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said first insulating film is made of a material selected from a group including silicon oxide, oxy-nitride and oxidized silicon nitride.

Claim 65 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said second insulating film is made of silicon nitride.

Claim 66 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said first insulating film contains a void.

Claim 67 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said interlayer insulating film contains a void.

Claim 68 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said portions of said first insulating film are embedded between said first memory cell gates or between said second memory cell gates to a height equal to a height of said first memory cell gates and said second memory cell gates.

Claim 69 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said portions of said first insulating film are embedded between said first memory cell gates or between said second memory cell gates to a height in a middle of a height of said first memory cell gates and said second memory cell gates.

Claim 70 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said portion of said first insulating film is provided on side surfaces of said one of said pair of first selecting gates and said one of said pair of second selecting gates.

Claim 71 (New): The method of manufacturing a semiconductor device according to claim 48, wherein a further portion of said first insulating film is formed on upper surfaces of said first memory cell gates and said second memory cell gates.

Claim 72 (New): The method of manufacturing a semiconductor device according to claim 48, wherein said contact electrode is formed in a self-align manner to said one of said pair of first selecting gates and said one of said pair of second selecting gates.

Claim 73 (New): A method of manufacturing a semiconductor device comprising:

forming a first gate electrode and a second gate electrode on a semiconductor substrate;

forming a first diffusion layer and a second diffusion layer under one and the other of opposite side portions of the first gate electrode, with the first gate electrode as a mask;

forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first gate electrode and said second gate electrode in such a manner that a portion of said first insulating film is embedded

between said first gate electrode and said second gate electrode to a height above a height of said first gate electrode, another portion of said first insulating film is provided on a major part of said first or second diffusion layer to a height lower than a height of said first gate electrode;

forming a second insulating film on said first insulating film;

forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film;

etching a portion of said first insulating film, a portion of said second insulating film and a portion of said interlayer insulating film, which are on said major part of said first or second diffusion layer, to form a contact hole leading to said major part of said first or second diffusion layer; and

embedding a conductive material in said contact hole to form a contact electrode connected to said major part of said first or second diffusion layer.

Claim 74 (Previously Presented): The method of manufacturing a semiconductor device 73, wherein a width of said first diffusion layer is larger than a width of said second diffusion layer.